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**Listing and Amendments to the Claims**

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (currently amended) A circuit arrangement comprising:  
a first circuit having an output line and an input line;  
a second circuit having an input line for receiving signals from the output line of the first circuit, and an output line for transmitting signals to the input line of the first circuit; and

a control circuit having input lines for receiving the signals from the output lines of the first and second circuits, the control circuit inhibiting the signals transmitted from the output line of the second circuit to the input line of the first circuit when the first circuit is transmitting signals to the input line of the second circuit and thereby preventing the second circuit from re-transmitting the signals received from the first circuit back to the first circuit and further preventing the first circuit from generating an interrupt signal; and

wherein the circuit arrangement is included in a television receiver.

2. (cancelled)

3. (cancelled)

4. (currently amended) The circuit arrangement of claim [[2]] 1, wherein the control circuit keeps the input line of the first circuit at a high state when the first circuit is transmitting signals to the input line of the second circuit.

5. (currently amended) The circuit arrangement of claim [[2]] 1 wherein the first circuit is a selected one of a Universal Asynchronous Receiver/Transmitter (UART) and a Universal Synchronous/Asynchronous Receiver/Transmitter (USART).

6. (original) The circuit arrangement of claim 5, wherein the second circuit is a G-Link circuit.

7. (currently amended) The circuit arrangement of claim ~~[[2]]~~ 1 wherein the second circuit further comprises a bi-directional line.

8. (original) The circuit arrangement of claim 7, wherein short-circuiting the bi-directional line initiates a demonstration mode.

9. (original) The circuit arrangement of claim 8 wherein the shorting circuiting is a short circuit to ground.

10. (previously presented) The circuit arrangement of claim 1 wherein the control circuit inhibits the signals transmitted from the output line of the second circuit to the input line of the first circuit when the first circuit is transmitting signals to the input line of the second circuit during a first mode of operation and allows the second circuit to transmit signals to the first circuit during a second mode of operation.

11. (previously presented) The circuit arrangement of claim 1, wherein signals transmitted from the output line of the first circuit control an external pager module through the second circuit for connecting to a pager service.

12. (previously presented) The circuit arrangement of claim 1, wherein the second circuit further comprises a second input line for receiving IR signals transmitted from an IR source and a second output line for transmitting the IR signals for remotely controlling an external device.

13. (original) The circuit arrangement of claim 1, wherein the second circuit provides feedback between the output line of the first circuit and the input line of the first circuit.

14. (previously presented) The circuit arrangement of claim 1 wherein the control circuit inhibits the signals transmitted from the output line of the second circuit to the input line of the first circuit according to a mode of operation.

15. (currently amended) A method for controlling communication from a serial interface circuit to a receiver-transmitter circuit in a system under control of a CPU and an operating system, the method comprising the steps of:

detecting a mode of operation of the system;

if the mode is a first mode, allowing the serial interface circuit to transmit signals to the receiver-transmitter circuit, wherein the serial interface circuit comprises a bi-directional line; and

if the mode is a second mode, detecting whether the receiver-transmitter circuit is transmitting signals to the serial interface circuit, and if the receiver-transmitter circuit is transmitting signals to the serial interface circuit, prohibiting the serial interface circuit from re-transmitting the signals received from the receiver-transmitter circuit back to the receiver-transmitter circuit and thereby preventing the receiver-transmitter circuit from generating an interrupt signal.

16. (previously presented) The method of claim 15 wherein the receiver-transmitter circuit is a selected one of a Universal Asynchronous Receiver/Transmitter (UART) and a Universal Synchronous/Asynchronous Receiver/Transmitter (USART).

17. (previously presented) The method of claim 15, wherein the serial interface circuit is a G-Link circuit.

18. (cancelled)

19. (currently amended) The method of claim ~~[[18]]~~ 15, wherein short-circuiting the bi-directional line initiates a demonstration mode.

20. (currently amended) The method of claim ~~[[19]]~~ 15, wherein the shorting circuiting is a short circuit to ground.

21. (new) A circuit arrangement comprising:  
a first circuit having an output line and an input line;

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a second circuit having an input line for receiving signals from the output line of the first circuit, and an output line for transmitting signals to the input line of the first circuit, the second circuit further comprising a bi-directional line; and

a control circuit having input lines for receiving the signals from the output lines of the first and second circuits, the control circuit inhibiting the signals transmitted from the output line of the second circuit to the input line of the first circuit when the first circuit is transmitting signals to the input line of the second circuit and thereby preventing the second circuit from re-transmitting the signals received from the first circuit back to the first circuit and further preventing the first circuit from generating an interrupt signal.

22. (new) The circuit arrangement of claim 21, wherein short-circuiting the bi-directional line initiates a demonstration mode.

23. (new) The circuit arrangement of claim 21, wherein the first circuit is one of a Universal Asynchronous Receiver/Transmitter (UART) and a Universal Synchronous/Asynchronous Receiver/Transmitter (USART).